

## IN THE CLAIMS

Please amend the claims as follows:

Patent claims

What is claimed is:

Claim 1 (Currently Amended) A method for generating a trigger signal (A) ~~according to the~~based on a current differential protection principle ~~in the case of when~~ a fault occurs on a section (E) of an electrical power supply system, ~~in which~~comprising:

- monitoring differential current values (id) ~~are monitored with regard to exceeding for a~~ predetermined lower limit value of the differential current (id) ~~(differential current limit value (igu)) and also with regard to exceeding and~~ stabilization current values (is) weighted with a characteristic curve factor (K), and

- generating the trigger signal (A) ~~is generated if positive results of the two instances of monitoring if the differential current values exceed the predetermined lower limit value and~~ stabilization current values and are present simultaneously, characterized in that

- calculating the differential current values (id) and the stabilization current values (is) ~~are~~ calculated with instantaneous values of the currents (i1, i2) detected at the section (E) of the electrical power supply system, ~~as instantaneous values,~~

- forming and checking a first measurement quantity (isd), which is proportional to ~~the~~ a differential quotient of the stabilization current (is) with respect to time, ~~is formed and checked~~ in an evaluation operation to determine whether ~~this the~~ the first measurement quantity (isd) exceeds ~~at the~~ a predetermined limit value of the differential quotient of the differential current with respect to time ~~(differential current quotient limit value (igd1),~~

- forming and checking a second measurement quantity (idd), which is proportional to ~~the~~ a differential quotient of the differential current (id) with respect to time, ~~is formed and checked in~~

a further ~~in another~~ evaluation operation to determine whether the second measurement quantity (~~idd~~) exceeds the differential current quotient limit value (~~igd1~~), and

- generating the trigger signal (A) ~~is generated~~ if the two evaluation forming an checking operations each produce a positive results result at the same time as the two instances of monitoring.

Claim 2 (Currently Amended) The method as claimed in claim 1, wherein ~~characterized in that~~

- a check is made to determine whether the first measurement quantity (~~isd~~) is greater than the second measurement quantity, and if so, the trigger signal is generated (~~idd~~), ~~and, if appropriate, the trigger signal (A) is generated.~~

Claim 3 (Currently Amended) The method as claimed in claim ~~1 or 2~~, ~~characterized in that 1, wherein~~ a check is made to determine whether the second measurement quantity (~~idd~~) exceeds the first measurement quantity (~~isd~~) weighted with ~~the~~ a characteristic curve factor and if so, the trigger signal is generated (~~K~~), ~~and, if appropriate, the trigger signal (A) is generated.~~

Claim 4 (Currently Amended) The method as claimed in ~~one of the preceding~~ claims, claim 1, wherein ~~characterized in that~~

- the smallest value (~~ismin~~) of the stabilization current (~~is~~) is determined in each case in a time range in which the first measurement quantity (~~isd~~) becomes less than zero,  
—— ~~its~~ the largest value (~~ismax~~) is determined in each case in a time range in which the first measurement quantity (~~isd~~) becomes greater than zero, and
- a check is made to determine whether the stabilization current (~~is~~) is greater than KMIN times the smallest value (~~ismin~~), where  $1 < KMIN < \sqrt{2}$ , and 0.5 times the value of the largest value (~~ismax~~), and,  
—— ~~if appropriate,~~ if so, the trigger signal (A) is generated.

Claim 5 (Currently Amended) The method as claimed in ~~one of the preceding claims,~~  
~~characterized in that~~ claim 1, wherein the trigger signal (A) is generated if the evaluation  
operations and the instances of monitoring ~~have yielded~~ yield positive results  $N_s$  times in  
succession, where  $N_s$  is freely selectable.

Claim 6 (Currently Amended) The method as claimed in claim 5,  
~~characterized in that~~ wherein in the absence of  $N_s$  results, the trigger signal (A) is generated  
when at least the instances of monitoring have produced positive results  $N_z$  times, where  $N_s \ll$   
 $N_z$ .

Claim 7 (Currently Amended) The method as claimed in ~~one of the preceding claims,~~  
~~characterized in that~~ claim 1, wherein in the absence of a trigger signal (A), an internal inhibit  
signal (B) is generated if — the first measurement quantity ( ~~$i_{sd}$~~ ) is greater than the limit value  
of this quantity ( ~~$i_{gd2}$~~ ),

— ~~furthermore and~~ the second measurement quantity ( ~~$i_{dd}$~~ ) is less than the instantaneous  
value - weighted with the  $k$  factor - of the first measurement quantity ( ~~$k \cdot i_{sd}$~~ ) and, at the same  
time, the instantaneous value of the stabilization current ( ~~$i_s$~~ ) is greater than

- a limit value ( ~~$i_{sh}$~~ ),
- a first reweighted limit value ( ~~$i_{dg}/k$~~ ),
- a second reweighted limit value ( ~~$1.5 \cdot i_{dg}$~~ ), and
- a comparison value calculated as mean value from previous values ( ~~$i_{rms}$  comparison value~~).

Claim 8 (Currently Amended) The method as claimed in claim 7,  
~~characterized in that~~ wherein after the generation of an inhibit signal, a trigger signal is  
generated ~~only~~ when the instances of monitoring and/or the instances of evaluation have  
produced a positive result at least  $N_z$  times.

Claim 9 (Currently Amended) A current differential protection arrangement for a section ~~(E)~~ of an electrical power supply system ~~having, comprising:~~

- a measured value preprocessing device ~~(MV)~~, in which respective differential current values ~~(id)~~ and stabilization current values ~~(is)~~ respectively assigned thereto are formed continuously from currents ~~(i1, i2)~~ detected at the ends of the section ~~(E)~~, having, the measured value preprocessing device is configured such that it generates differential current instantaneous values and stabilization current instantaneous values;

- an evaluation device ~~(AW)~~ connected downstream of the measured value preprocessing device ~~(MV)~~, ~~————~~ in which evaluation device the differential current ~~(id)~~ is checked to determine whether it exceeds a predetermined differential current limit value ~~(idg)~~, ~~and having;~~

- a logic circuit ~~(L1)~~, which, on the input side, is connected to the evaluation device ~~(AW)~~ and has an output for outputting a trigger signal ~~(A)~~;<sub>2</sub>

~~characterized in that~~

~~the measured value preprocessing device (MV) is designed in such a way that it generates differential current instantaneous values and stabilization current instantaneous values (is);~~

~~———— a first limit value stage (Gs) is~~

~~———— a first limit value stage arranged downstream of a first a first differentiator (Ds), to which, to which stabilization current instantaneous values (is) are applied, which limit value stage is also, which limit value stage is connected to a a differential current quotient limit value transmitter (G1) on the the input side;~~

~~———— a second limit value stage (Gd) is arranged downstream of a second differentiator (Dd), to which; and~~

a second limit value stage arranged downstream of a second differentiator, to which differential current instantaneous values are applied, which limit value stage is also connected to the differential current quotient transmitter (G19) on the input side, and, which limit value stage is connected to the differential current quotient transmitter on the input side, wherein

- the logic circuit ~~(L1)~~ is arranged downstream of the limit value stages and generates the trigger signal ~~(A)~~ when output signals of the limit value stages are present.

Claim 10 (Currently Amended) The current differential protection arrangement as claimed in claim 9,  
~~characterized in that~~ further comprising a first comparator (K1) is connected to the two differentiators (~~De, Ds~~) and, on the output side, is connected to the logic circuit (~~L1~~).

Claim 11 (Currently Amended) The current differential protection arrangement as claimed in claim ~~7 or 8~~,  
~~characterized in that~~ 7. further comprising a second comparator (K2) is indirectly arranged downstream of the first differentiator (~~Ds~~) via a translation stage (~~U1~~) and of the second differentiator (~~De~~) and is connected to the logic circuit (~~L1~~) on the output side.

Claim 12 (Currently Amended) The current differential protection arrangement as claimed in ~~one of claims 9 to 11~~ claim 9, wherein  
~~characterized in that~~

~~provision is made of~~ a determination device (U) for the smallest value (~~ismin~~) of the stabilization current (~~is~~) provided,

- a weighting device (BE) is connected to the determination device (U), and
- a comparison stage (VS) is arranged downstream of the weighting device (~~BE~~), to which comparison stage, on the input side, the stabilization current instantaneous values (~~is~~) are also applied and which comparison stage is connected to the logic circuit (~~L1~~) on the output side.

Claim 13 (Currently Amended) The current differential protection arrangement as claimed in ~~one of claims 9 to 12~~ claim 9, further comprising:

~~characterized in that~~

- a first comparison stage (V1) is arranged downstream of a transmitter (G1g) for the differential current quotient limit value (~~idg~~) and a second transmitter (G2) for the stabilization quotient limit value (~~igf~~), which comparison stage is connected to the logic circuit (~~L1~~) on the output side,

- a ~~further~~second comparison stage ( $V2$ ) is connected, on the input side, ~~on the one hand~~ to the input of the first differentiator ( $Ds$ ) and ~~on the other hand~~, via a ~~further~~another translation stage ( $U2$ ), to a transmitter ( $G1g$ ) for the limit value ( $idg$ ) of the differential current ( $id$ ) and is connected to the logic circuit ( $L1$ ) on the output side,
- a third comparison stage ( $V3$ ) is connected, on the input side, ~~on the one hand~~ to the output of the first differentiator ( $Ds$ ) and ~~on the other hand~~ to the output of the ~~further~~another transmitter ( $G2$ ) and is connected to the logic circuit ( $L1$ ) on the output side,
- a fourth comparison stage ( $V4$ ) is connected, on the input side, ~~on the one hand~~ to the input of the second differentiator ( $Dd$ ) and ~~on the other hand~~, via a third translation stage ( $U3$ ), to the input of the first differentiator ( $Ds$ ) and is connected to the logic circuit ( $L1$ ) on the output side, and
- a fifth comparison stage ( $V5$ ) is connected, on the input side, ~~on the one hand~~ to the output of the second differentiator ( $Dd$ ) and ~~on the other hand~~, via a fourth translation stage ( $U3$ ), to the output of the first differentiator ( $Ds$ ) and is connected to the logic circuit ( $L1$ ) on the output side.